```
PIN  22   CS_CHAR   COMBINATORIAL ; OUTPUT char gen chip select
PIN  23   CS_CHARD     REGISTERED ; OUTPUT delayed CS_CHAR
PIN  24   VCC

;---------------------------- Boolean Equation Segment -------------

EQUATIONS

/CS_ROM = /A19 * /AS

/CS_RAM = A19 * /A18 * /A17 * /AS

/CS_SPARE = A19 * /A18 * A17 * /AS

/CS_EXT = A19 * A18 * A17 * A16 * /AS
        + /CS_SPARE

/IACK = FC0 * FC1 * FC2 * /AS

DTACKDLY = /CBLANK * DTACKDLY * /AS
         + AS

/DTACK = /AS * /FC0 * CS_CHARI
       + /AS * /FC1 * CS_CHARI
       + /AS * /FC2 * CS_CHARI
       + /DTACKDLY * /CS_CHARI

CS_WAVE = CS_WAVEI

CS_CHAR = CS_CHARI + DTACKDLY

CS_CHARD = CS_CHAR


;---------------------------- Simulation Segment --------------------

SIMULATION


TRACE_ON FC0 FC1 FC2 IACK AS 8M CS_CHARI CS_CHAR DTACKDLY DTACK CBLANK

SETF /AS /FC2 /FC1 /FC0 A19 /A18 /CBLANK CS_CHARI CS_WAVEI

CLOCKF 8M
SETF  /AS /FC2 FC1 /FC0

CLOCKF 8M
SETF  /AS FC2 /FC1 /FC0

CLOCKF 8M
SETF  /AS FC2 FC1 /FC0

CLOCKF 8M
SETF  /AS FC2 FC1 FC0

CLOCKF 8M
SETF AS FC2 FC1 FC0

CLOCKF 8M
SETF /AS /FC2 /FC1 /FC0 A18 /CS_CHARI

CLOCKF 8M
SETF /AS
```